Application of Reconfigurable Logic Technology to Intelligent Human Sensing

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This paper presents our recent progress on the application of reconfigurable logic technology to intelligent human sensing. First, hardware specialization technique is presented to realize small and fast preprocessor based on reconfigurable logic devices. Second, a load balancing technique for heterogeneous systems is introduced. Then, a real-time aberration correction system for scanning transmission electron microscope is presented as a possible application of our sensor information processing system.

1. Introduction

Huge numbers of sensors are involved in the intelligent human sensing system. These sensors continuously yield enormous amounts of data that must be processed without delay since it is both impossible and futile to record it all. Since these data are generated by sensor hardware, their format is relatively simple and fixed. Custom hardware is well suited to process such large amounts of simple data rapidly, whereas it is impractical to handle them by microprocessors that are intrinsically sequential and weak in bulk data transfer. Even the recent high-performance microprocessors cannot escape from the bandwidth limitation between processor and memory (*von Neumann bottleneck*). For sensor preprocessing, it is natural to adopt a hierarchical design, which includes a central processing unit and low-level preprocessors. Figure 1 illustrates the concept of reconfigurable sensor preprocessors [1].

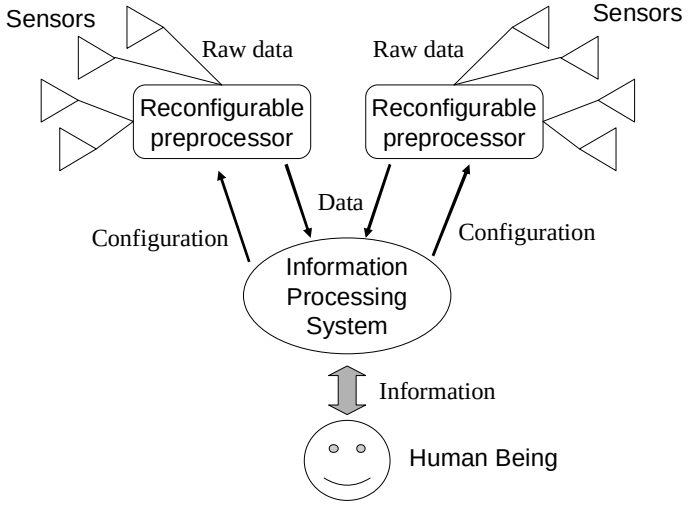


Fig.1 Reconfigurable logic for intelligent human sensing [1]

One of the possible problems is that custom preprocessors are less elastic than software in supporting various applications. However, we can adopt a dynamically reconfigurable circuit, which is flexible in adapting to each application. A reconfigurable logic device is a kind of LSI that can change its logic function (configuration) at run-time. Using reconfigurable devices, we can reprogram the device as if to

change the software. Field Programmable Gate Array (FPGA), which is a kind of reconfigurable logic device, can now deliver 1—10 million gates at a reasonable price. The design cost would not be a major concern, because sensor outputs are rather simply formatted and thus the design of sensor preprocessor would not be complicated. In the following discussions, the author introduces the possibilities of reconfigurable logic preprocessors.

2. Hardware Specialization with Reconfigurable Circuits

In the previous paragraph, we discussed customizing logic circuits for an application or an algorithm. However, it is possible to customize the circuit for specific input data. This technique is called *hardware specialization* or *data-dependent circuit*. The basis of hardware specialization is as follows: If any input of a logic gate is fixed to a constant, that gate is eliminated, and the corresponding constant propagates to the output of that gate. Figure 2 illustrates some examples of this. Such reduction is recursively applicable, consequently reducing many combinatorial gates and flip-flops. The derived circuit will operate at a higher frequency because the length of the critical path is also reduced. It naturally avoids the von Neumann bottleneck, because input data are not located in memory but built in the logic circuit. The obvious drawback of this technique is that (1) it requires circuit generation for each input data, and that (2) it requires reconfigurable devices for implementation. Sensor preprocessors are supposed to locate near the sensors to process raw data very fast with minimal hardware and power consumption. Therefore, hardware specialization is well suited for sensor preprocessors; e.g., the event detector to find a specific event, the comparator with a specific threshold, etc.

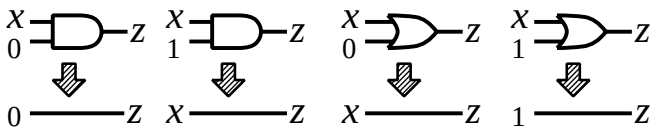


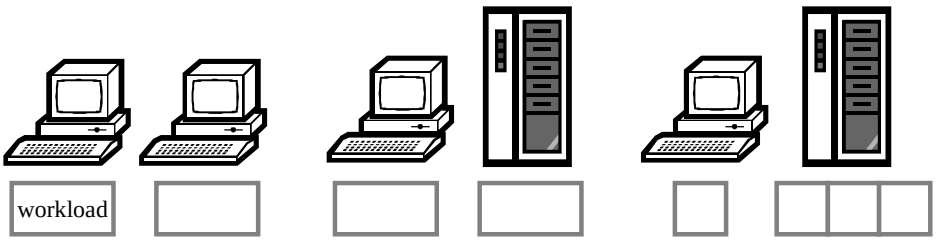
Fig.2 Logic reduction in hardware specialization

The author has been studied the custom circuit for subgraph isomorphism problems, which are a kind of pattern match problem. It has various important applications, while generally being NP-complete. Though Ullmann [2] and Konishi [3][4] proposed the custom circuit designs to accelerate subgraph isomorphism problems, they require many hardware resources for large problems. The author examined the design of data-dependent circuits for subgraph isomorphism problem, and reported the evaluation results on an actual FPGA platform. The circuits were implemented on a Xilinx XC2V3000 FPGA, and they successfully operated at clock frequency 25 MHz. In the case of graphs with 16 vertices, the execution time was about 1/40 of the software executed on an up-to-date microprocessor (Athlon XP 2600+ of 2.1 GHz clock). Even if the circuit generation time is included, data-dependent circuits were about 28 times faster than the software for random graphs with 16 vertices. This performance advantage becomes larger for larger graphs. Two algorithms (Ullmann's and Konishi's) were examined, and the data-dependent approach was found to be equally effective for both algorithms. We also examined two types of input graph sets, and found that data-dependent approach shows advantage in both cases. More details will be found in the references [5]—[9].

3. Load Balancing for Heterogeneous Systems

Sensor information processing system (shown in Fig.1) inevitably becomes a heterogeneous system. Heterogeneous systems are flexible and cost-effective, but entail intrinsic difficulties in optimization. An example of this is shown in Fig.3. In a homogeneous system, the workload is equally distributed among processors (Fig.3 (a)). However, if this is done in a heterogeneous system, the system performance is

degraded by load imbalance (Fig.3 (b)). Since fast processors (right) finish their jobs earlier, they have to wait for slow processors (left) to finish their jobs. To maximize the system performance, workload must be distributed according to the performance of each processor.



(a) Equal distribution (b) Load imbalance (c) Multiprocessing

Fig.3 Load balancing for heterogeneous systems

Although it is simple to invoke multiple processes on fast processing elements (PEs) to alleviate load imbalance (Fig.3 (c)), the optimum process allocation is not so obvious. Communication time is another problem. It is sometimes better to exclude slow PEs to avoid performance degradation, but it is generally difficult to find the optimal PE configuration. The authors modeled this problem as a mathematical programming problem, taking both the communication time and the calculation time into consideration. This problem is treated as a combinatorial optimization problem to be solved so as to make the total execution time optimal. In the authors' scheme, the execution time is first modeled from the measurement results of various configurations. Then, the derived model is used to estimate the optimal PE configuration and process allocation. The authors implemented the models from HPL (High Performance Linpack benchmark) of small problem size N, and estimated the optimal configuration for various N. The estimated best configuration and the estimated execution time were not far from the actual best configuration and the actual best execution time. More information will be found in the references [10]—[14].

4. Real-time Aberration Correction for Scanning Transmission Electron Microscope

The resolution of a scanning transmission electron microscope remains 100 times worse than its theoretical limit owing to the spherical aberration of objective lens. Ikuta [15] proposed a system to generate an aberration-free amplitude image and phase image using multiple small detectors with signal processing. Figure 4 illustrates the concept of Ikuta's aberration correction system. The image of object is captured by the array of small detectors, each of which generates a 2D digital image. Each image is processed by 2D-FFT, 8-shaped band-pass filter, and 2D-IFFT in *Signal Processing* stage of Fig.4. The aberration-free image is derived by summing up all these processed images.

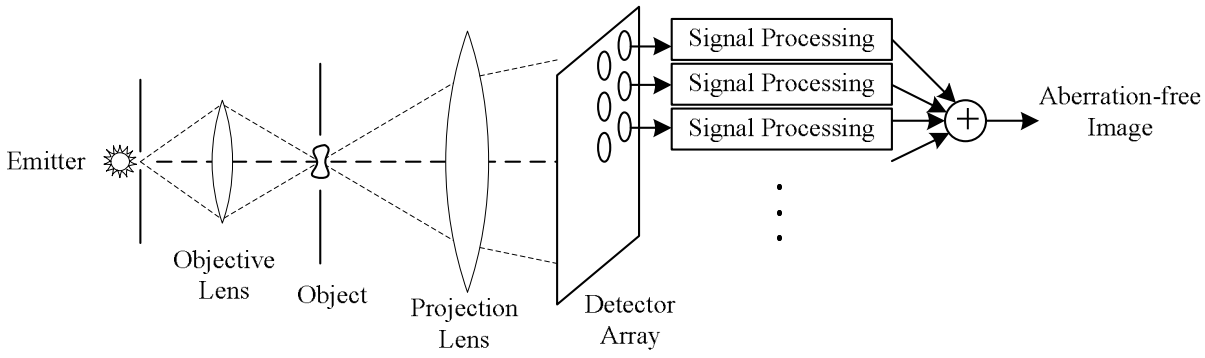


Fig.4 The block diagram of a real-time aberration correction system for scanning transmission electron microscope

Ikuta’s system is a good example of actual sensor information systems. The authors [16] optimized the performance of this signal processing stage, and estimated the overall performance of Ikuta's aberration correction system. These experiences would be applicable to other sensor information systems, which are now under development in our COE program.

5. Conclusion

The authors are currently working on a sensor-actuator system, which includes a real-time control circuit. A simple prototype of reconfigurable preprocessor is to be implemented in this system for preliminary evaluations. The first evaluation results will come up before April 2005.

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