DATE：2023/12/1

Department of Electrical and Electronic Information Engineering		ID	203230
Name	Takuto Shoji		

Supervisor	Shuichi Ichikawa

Abstract

Title	Study of image processing circuits by Stochastic Computing

In recent years, due to the increase in the amount of information in the fields of artificial intelligence and image processing, design methods that are advantageous in reducing the circuit area have been attracting attention. Stochastic computing (SC) is a design method to reduce circuit area, where arithmetic operations can be implemented with simple logic circuit.

Ichihara et al. and Salehi proposed a method to reduce the circuit area by sharing a linear feedback shift register (LFSR) between two SN generators (SNG). Ichihara et al. and Salehi proposed a method to shuffle the output of an LFSR to generate two SNs from a single LFSR. This study presents a method of inserting a NOT gate in addition to the shuffling.

Li et al. implemented a digital image processing algorithm and evaluated its error tolerance, hardware resources, and latency. They found that the latency increases when SC is used. Chen and Li proposed AFE to achieve low latency and low area occupancy.

Inotani extended the AFE and proposed a method for flattening multi-bit stream, which is implemented in edge detection and Gaussian filter. It is expected that the flattening method can converge the computation results within a short bit length. However, as the evaluation of Inotani is still insufficient, I conducted a detailed evaluation again in this study. In this study, edge detection circuits and Gaussian filters were designed and their absolute mean errors (MAE) were measured using the following four methods. (1) AFE (default) proposed by Chen and Li, (2) AFE (flattening) for flattening multi-bit stream, (3) SC (default) without sharing LFSR, and (4) SC with shared LFSR by shuffling random bit stream or inserting SC (with NOT gate). SIDBA registered images (airplane, baboon, barbara, bridge, peppers, and sailboat) were used as input images. In addition, I evaluated the hardware resources by logic synthesis.

For edge detection and Gaussian filter, the images generated from AFE (default) and SC (with NOT gate) were not significantly different from those generated from pixel values obtained by floating-point operations (expected values). This indicates that the two methods have sufficient practical performance in terms of MAE.

The hardware resources for AFE (default), SC (default) and SC (with NOT gate) were measured. For both the Gaussian filter and edge detection, SC (with NOT gate) is found to have a smaller logic size than AFE (default). Since the two methods have sufficiently practical performance in terms of MAE, I conclude that SC (with NOT gate) is effective because of its smaller logic size.