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Abstract

Title	An Experimental Implementation of Stochastic Image Processing Application by Amplitude and Frequency Encoding

Many fields, such as image processing and machine learning, do not require high accuracy, where approximate computation is attracting attention. Stochastic computing (SC), a type of approximate computation, uses a stochastic bitstream (SB) and is considered as a computation method with strong soft-error tolerance and an area-efficient implementation. Li et al. (2014) implemented a digital image processing algorithm as an application circuit for SC but they encountered problems such as large latency. Chen and Li (2022) proposed Amplitude and Frequency Encoding (AFE), a new coding scheme that extends SC to achieve both low latency and low area.

In this study, two image processing circuits, i.e., an edge detection circuit and a Gaussian filter, were implemented using AFE, and their accuracy was evaluated. AFE performs operations using multi-bit streams instead of SB. Since the multi-bit stream adds magnitude (Amplitude, a) to the 0s and 1s of the SB used in conventional SC, the derived stream consists of the series of 0 and a. This study proposes to flatten the multi-bit stream to improve accuracy. We proposed an implementation with fixed point representation, where the fractional part of the flattened value is represented by SB. Mean absolute error (MAE) was used as a measure of accuracy. The C language was used for the source code, and the input precision was set to 8 bit. SIDBA registered images (airplane, baboon, barbara, bridge, lena, peppers, sailboat) converted to black-and-white PGM format were used as input images, with a resolution of 256×256 pixels.

The edge detection circuit and Gaussian filter were implemented, and MAE was compared for each method. The smallest error was observed when the stream length was set to 16 bits with fractional implementations of both the edge detection circuit and the Gaussian filter. Compared to the AFE-based implementation, the edge detection circuit and the Gaussian filter were reduced by 21.0% and 76.4%, respectively. As the number of cycles was varied, the edge detection circuit had a smaller error when the number of cycles was larger than 256, and the Gaussian filter had a smaller error when the number of cycles was larger than 32 bits. Future work includes high-level synthesis of edge detection circuits and Gaussian filters using Vivado HLS to evaluate hardware resources and performance.